SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Appln. Of:	TAKANO et al.
Appln. No.:	10/648,995
Filed:	August 27, 2003
For:	Semiconductor Integrated Circuit Having Logic Circuit...
Docket:	NEC OSP-9770 DIV II

Received:

1. Supplemental Information Disclosure Statement (2 pgs)
2. Copy of U.S. Office Action (9 pgs)
3. PTO Form 1449 (1 pg)
4. 5 Cited References

1/6/04 kmg

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/357,752	02/04/2003	Susumu Takano	NEC OSP-9770 DIV	7035

7590 10/01/2003

EXAMINER
AUDUONG, GENE NGHIA

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/01/2003

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3 mos. 11/1/03 2/1/04
12/1/03 3/1/04
1/1/04 4/1/04

Please find below and/or attached an Office communication concerning this application or proceeding.

dlk.

Office Action Summary	Application No.	Applicant(s)	
	10/357,752	TAKANO ET AL	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) *2-4 and 6-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *2-8* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *Feb-03* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 and 5, drawn to a semiconductor integrated circuit, classified in class 365, subclass 51.

   II. Claims 2-4 and 6-8, drawn to semiconductor circuit having particular connection for a logic circuit, classified in class 365, subclass 63.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars elements and their connection as claimed in the subcombination because each of the logic circuit in Group II having its particular structure and connection. The subcombination has separate utility such as an AND type logic or NOR type logic circuit to generate a particular output based on the specific input logic signals for use in the device and each of the logic circuit having its own structure and connection.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. This application contains claims directed to the following patentably distinct species of the claimed invention: Group II, claims 2 and 6 claiming the particular logic circuit for figure

1A; claims 3 and 7 claiming the particular logic circuit for figure 10A; and claims 4 and 8 claiming the particular logic circuit for figure 11A. Each of the logic circuit having each own structure.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

5. During a telephone conversation with Norman Soloway on August 26, 2003 a provisional election was made without traverse to prosecute the invention of Group I, claims 1 and 5. Affirmation of this election must be made by applicant in replying to this Office action. Claims

2-4 and 6-8 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

6. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

7. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/741,304, filed on December 19, 2000.

Drawings

8. Figure 12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoeli (U.S. Pat. No. 5,138,194).

Regarding claim 1, Yoeli discloses an integrated logic circuit comprises: one or more first transistors for supplying electric charges to an external load via an output terminal (figure 4, one or more P-type transistor for applying electric charges (pull-up) to an external load via an output pad); and one or more second transistors for drawing electric charges from the load via the output terminal (N-type transistor for drawing electric charges from the load (pull-down), and wherein: in the logical operation of the logic circuit, the above supply and drawing of electric charges are executed according to combination of the states of a plurality of binary logic signals input from an external device (the electric charges are executed according to combination of the logical states of the input signals OE, D); and among all the transistors in the logic circuit, each transistor other than the first transistors for supplying electric charges has a threshold voltage value lower than that of each first transistor (P-type pull-up transistor 24 has a threshold voltage value higher than that of each P-type transistor in the circuit; see figure 4, col. 2, lines 61-66; col. 4, lines 50+).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoeli (U.S. Pat. No. 5,138,194).

Regarding claim 5, Yoeli discloses an integrated circuit having all of the limitation as claimed in claim l. Yoeli does not specifically disclose wherein the logic circuit is applied to a

decoder circuit. However, a logic circuit to generate an output signal (control signal) according to combination of the states of the input logic signals then applying to a next stage, command decoder, read/write control circuit, or any other control circuit to perform a specific function as desired for a specific need by the designer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yoeli's device to further claiming the logic circuit is applied to a decoder circuit as claimed to decode and generate a particular control signal for the memory device as needed for the circuit.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
August 29, 2003

Gene N Auduong
Examiner
Art Unit 2818